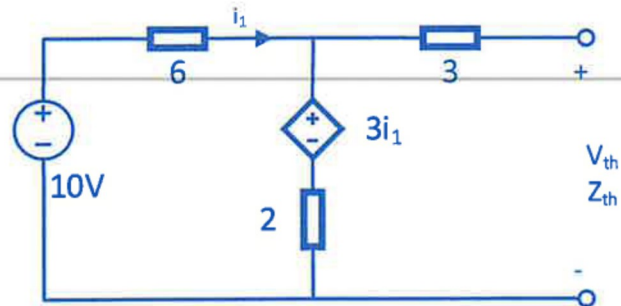


For the circuit shown below



- (a) Calculate the Thevenin voltage (V_{TH}).
(b) Calculate the Thevenin impedance (Z_{TH}).

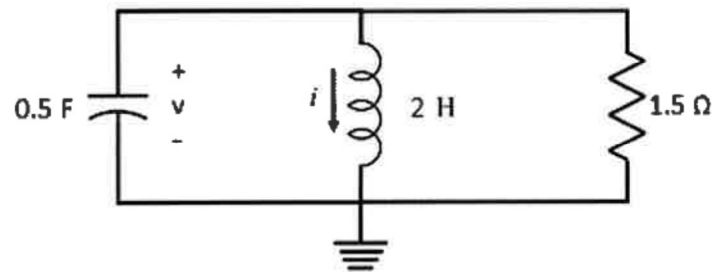
Problem : Q2

Area: Circuits/Electronics

Student Code: ____

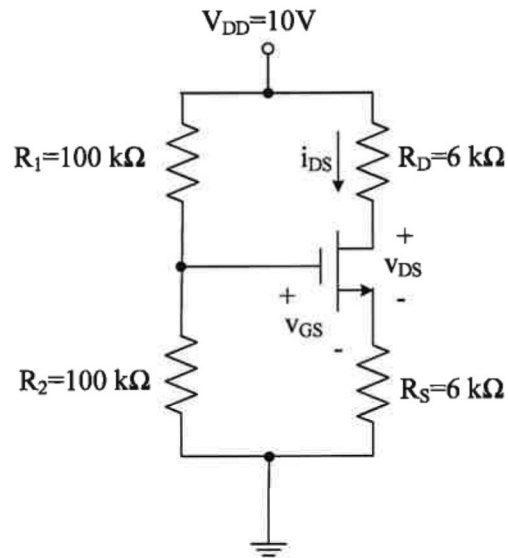
For the following circuit,

- a) Determine the Source-Free response, $v(t)$, for $t > 0$. Let $i(0) = 5$ A, $v(0) = 100$ V.



- b) Is the circuit (Overdamped \ Critically Damped \ Underdamped – Circle One)?

Consider an n-channel enhancement-mode MOSFET with a threshold voltage of $V_{on} = 1\text{V}$ and $K=1\text{ mA/V}^2$. Find the operating point v_{DS} and i_{DS} and verify whether the transistor is operating in the saturation or in the triode (linear) region.



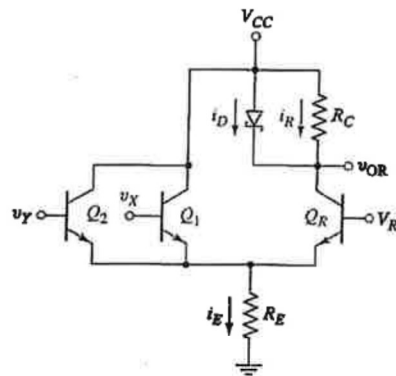
Problem: Q4

Area: Circuits/Electronics

Student Code _____

Consider the following ECL logic gate with Schottky diode with $V_{CC} = 1.7 \text{ V}$ and $R_E = R_C = 8 \text{ k}\Omega$.

Assume $V_\gamma = 0.4 \text{ V}$ and $V_{BE}(\text{on}) = 0.7 \text{ V}$. Calculate the current through the Schottky diode when max current flows through R_C .



Global navigation satellite systems (GNSS) have multiple satellites that orbit the Earth. Each satellite transmits radio signals, which can be picked up by radio receivers on the surface of the Earth, aircraft, and low Earth orbit satellites. After collecting signals from multiple satellites, the radio receivers can calculate the time of day, and the distance to each satellite. They can then reference tables that describe the orbit of the satellites, to triangulate their position.

In the USA the best known GNSS is the Global Positioning System (GPS), operated by the US government. The Russian government operates the Global Navigation Satellite System (GLONASS). China is deploying the BeiDou Navigation Satellite System (BDS), and the European Union is deploying the Galileo GNSS system.

By the time the GNSS signals reach the ground, they have a very low power density (very few watts per square meter). This makes it difficult for GNSS receivers to detect the signals, and the systems prone to interference from ground-based transmitters operating at the same frequency. Since every modern phone has a GNSS receiver in it, any interference with their signals will be quickly detected, and automatically reported through the global telephone network. If you design or operate electronic equipment, it is important that you do not intentionally, or unintentionally, interfere with GNSS signals (unless that's your job/mission).

Here is a list of frequencies used by the various systems

1191.80 MHz – BDS and Galileo
1227.60 MHz – GPS
1246.00 MHz – GLONASS
1268.52 MHz – BDS
1575.42 MHz – GPS, BDS and Galileo
1602.00 MHz – GLONASS
2492.03 MHz – BDS

Electronic equipment, such as computers, sometimes unintentionally transmit radio signals. This is particularly true for systems that use digital signals with short rise/fall times. Perfect grounding and shielding would theoretically prevent your system from radiating these signals, but imperfections in the design and manufacture of the equipment means that every sine wave you generate will – to some degree – radiate out of your device. If you don't want to radiate at X Hz, never generate sine waves at X Hz.

You are designing a digital logic circuit, which uses a square wave as a clock signal. You can assume this is a perfect square wave, with very short rise/fall times, and a 50% duty cycle. Answer all three questions below.

- A) You are allowed to select the clock frequency, but it must be between 400 MHz and 500 MHz. Are there any frequencies in this range you suggest avoiding?
- B) Repeat part A, but for clock frequencies from 600 MHz to 650 MHz.
- C) Repeat part A, but for clock frequencies from 2 GHz to 2.4 GHz.

For full credit, you must list not only the problem frequencies, but give a brief justification of why the frequency is a problem.

When you have two options, which one is superior often depends on your point of view. If you like to drive fast, then a sports car is superior to a mini-van. But if you need to transport your daughter's soccer team to practice, the mini-van looks like the better choice because it holds more people and cargo.

Each item below lists two different types of digital modulation. For each pair, give one reason why the first modulation is superior to the second, and one reason why the second modulation is superior to the first.

For example, if the modulation schemes are called COOK and BOOK, you might say: COOK is superior because it uses less transmitted power for a given error rate, while BOOK is superior because it uses less bandwidth for a given data rate.

If you think a modulation like COOK has no advantage over BOOK, then simply state that COOK is inferior in every way.

You do not have to mathematically prove, or justify, any of your claims – but if you want to add an explanation, that's OK.

- A) OOK vs. BPSK (on/off keying versus binary phase shift keying)
- B) BPSK vs. QPSK (binary phase shift keying versus quadrature phase shift keying)
- C) QPSK vs. QAM (quadrature phase shift keying versus quadrature amplitude modulation)
- D) QPSK vs BFSK (quadrature phase shift keying versus binary frequency shift keying)

Problem : 10**Area: Controls****Student Code_____**

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Consider the third-order system with the differential equation

$$\frac{d^3 y}{dt^3} + 5 \frac{d^2 y}{dt^2} + 3 \frac{dy}{dt} + 2y = u.$$

- (a) (30% of score) Determine the state variable representation.
- (b) (70% of score) Design a state feedback gain matrix K if we seek a rapid response to a low overshoot, and a settling time of 1 second with $\omega_n = 6$.

Problem: 13**Area: Power****Student Code: _____**

Consider an induction motor with the following specifications: 4-pole, 230 V, 60 Hz three-phase, $R_1 = 0.12 \, \Omega$, $R_2 = 0.26 \, \Omega$, $X_1 = 1.5 \, \Omega$, $X_2 = 1.1 \, \Omega$, $X_m = 8.1 \, \Omega$, slip at rated torque 0.03. We will be using this motor instead on a **50 Hz** system.

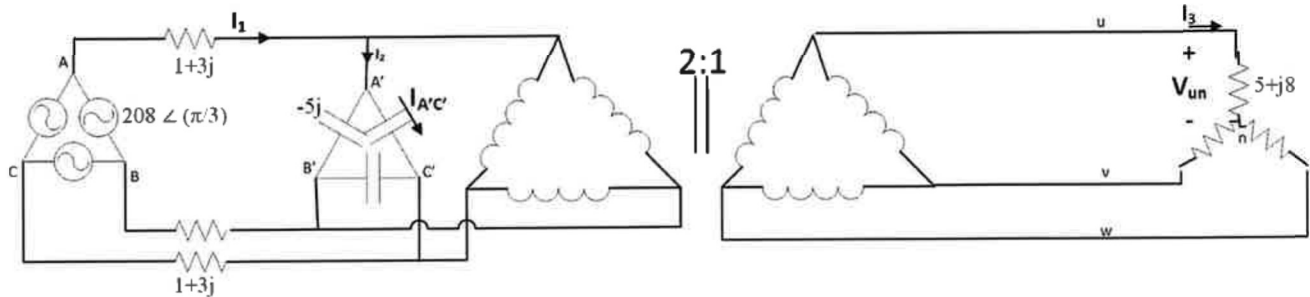
- a) Draw the 50 Hz per-phase equivalent circuit with all impedances labeled NUMERICALLY.
- b) Determine the appropriate source voltage to maintain constant flux density.
- c) Determine the synchronous speed, in RPM and rad/s.
- d) On a 60 Hz source, the rated slip is 0.03, which corresponds to some speed $n_{60, \text{rated}}$ (in RPM) and some rotor electrical frequency, $f_{re, \text{rated}}$. For a 50 Hz source, at what new speed $n_{50, \text{rated}}$ (in RPM) will the rotor electrical frequency match $f_{re, \text{rated}}$? To be clear, your answer should just be $n_{50, \text{rated}}$.

Problem:14**Area: Power****Student Code: _____**

In the following circuit, find the following (both amplitude and angle):

Note: All elements are balanced positive sequence 3phase.

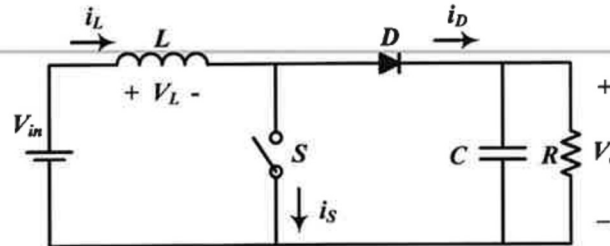
- a) I_1, I_2 , and I_3 (45 points).
- b) $I_{A'C'}$ (Capacitor current) (15 points).
- c) Phase voltage of the load $(5+8j)$ equal to V_{un} (15 points).
- d) 3-phase complex power of the source (15 points)
- e) 3-phase complex power of the capacitor bank. (10 points)



Problem 15**Power**

Code # _____

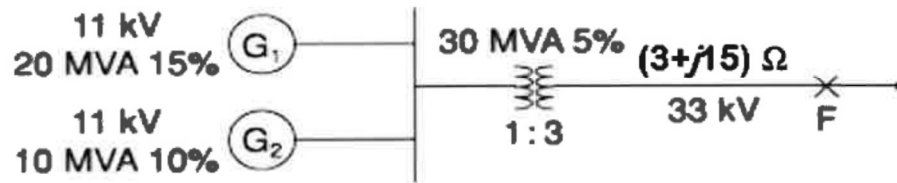
A Boost dc-dc converter has the following parameters: $V_{in} = 400$ V, $d = 0.25$, $V_{out} = 650$ V, $L = 100$ μ H, and $f_{sw} = 100$ kHz.



- a) Find the peak value of the inductor current. (20 points)
- b) Accurately plot the waveform of the inductor current. (20 points)
- c) Find the average value of the inductor current. (20 points)
- d) Find the input power. (20 points)
- e) Find the value of the load resistor. (20 points)

Problem: 16**Area: Power****Student Code: _____**

In the system shown below, a three-phase short circuit occurs at point F. Assume that prefault currents are zero and that the generators are operating at rated voltage. Choose base MVA as 30 MVA and the base line voltage at the HV-side of the transformer to be 33kV. Determine the fault current in per unit.

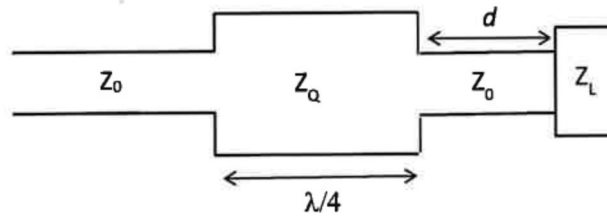


Problem : 17**Area: Waves & Devices****Student Code:_____**

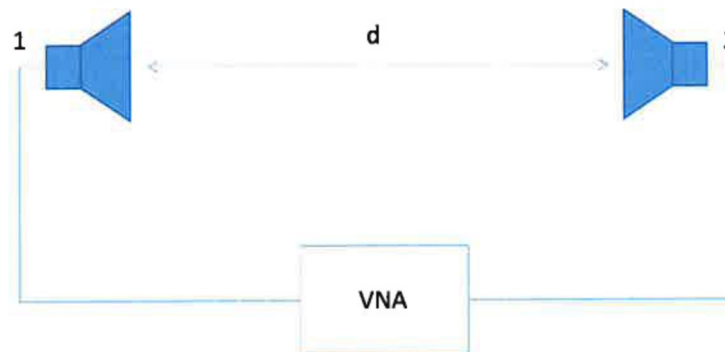
Uniform plane wave. Consider a uniform plane wave traveling in the z-direction in a simple lossless nonmagnetic medium (i.e., $\mu = \mu_0$) with a y-directed electric field of maximum amplitude of 60 V/m. If the wavelength is 20 cm and the velocity of propagation is 10^8 m/s, (a) determine the frequency of the wave and the relative permittivity of the medium and (b) write complete time-domain expressions for both the electric ($\vec{E}(z,t)$) and magnetic ($\vec{H}(z,t)$) field components of the wave.

Design a quarter wave transformer to match a load impedance of $Z_L = 73 + j42.5 \, \Omega$ to a transmission line of $Z_0 = 75 \, \Omega$. Indicate the location, d , along the line where the quarter wave transformer must be placed, along with the impedance of the quarter wave section, Z_Q .

This problem may be solved using traditional transmission line equations or by using the attached Smith Chart.



A measurement of the transmission coefficient between two identical antennas is performed in an anechoic chamber as shown in the figure below.



Assuming that the calibration of the vector network analyzer is performed at the antenna connectors (ports 1 and 2), the distance between the antennas is $d=3$ m, and the measured value of the transmission coefficient $|S_{21}| = -12$ dB at 1 GHz: 1) determine the gains of the antennas, 2) determine the effective antenna apertures, 3) calculate the amplitude of the electric field at the location of the antenna 2 if 0 dBm of power is applied to the input of the antenna 1.

Useful formulas:

1. Friis transmission equation:

$$\frac{P_r}{P_t} = G_t G_r \left(\frac{\lambda}{4\pi d} \right)^2$$

or

$$\frac{P_r}{P_t} = \frac{A_r A_t}{d^2 \lambda^2}$$

where P_t is the power fed to input of the transmitting antenna, P_r is the power available at the receiving antenna output, G_r is the gain of the receiving antenna, G_t is the gain of the transmitting antenna, A_r is the effective aperture of the receiving antenna, A_t is the effective aperture of the transmitting antenna, d is the distance between antennas, λ is the wavelength.

2. Effective antenna aperture is defined as

$$A_e = \frac{P_0}{S}$$

where P_0 is the power delivered by the receiving antenna to the load, and S is the power density of the electromagnetic field at the antenna location.

Problem : 20**Area: Waves & Devices****Student Code:_____**

- I. An abrupt silicon p-n junction has a net acceptor concentration 10^{19} cm^{-3} in the p-side and a net donor concentration 10^{16} cm^{-3} in the n-side, respectively. Answer the following questions assuming all dopants are ionized at room temperature (i.e. 300 K).
- [35%] Calculate the potential difference at thermal equilibrium (i.e. contact potential or built-in potential) across the depletion region (or space charge region) of the junction.
 - [10%] Calculate the potential difference across the junction when a reverse bias (- 0.5 V) is applied.
 - [10%] Describe the difference, in terms of physical meaning or definition, between the contact potential (in the problem a) and the diode turn-on voltage (e.g. the typical default 0.7 V for silicon p-n diode) (no more than two sentences or ~40 words).
- II. Consider a silicon sample doped with donors (10^{14} cm^{-3}) at room temperature. Excess carriers by photon absorption (steady-state concentrations of $2.0 \times 10^{13} \text{ cm}^{-3}$ electrons and $2.0 \times 10^{13} \text{ cm}^{-3}$ holes) are generated during a light illumination. Answer the following questions assuming electron mobility = $1,500 \text{ cm}^2/\text{V}\cdot\text{sec}$ and hole mobility = $500 \text{ cm}^2/\text{V}\cdot\text{sec}$, respectively.
- [25%] Calculate the conductivity of the sample without illumination.
 - [10%] Calculate the conductivity of the sample during illumination.
 - [10%] Discuss a possible application of this sample (no more than one sentences or ~20 words).

Constants*	Equations*
<ul style="list-style-type: none"> Elementary charge = $1.6 \times 10^{-19} \text{ [C]}$ $kT = 0.0259 \text{ [eV]}$ (at 300 K) Intrinsic concentration = $9.65 \times 10^9 \text{ [cm}^{-3}\text{]}$ (for silicon at 300 K) 	<ul style="list-style-type: none"> $n_o p_o = n_i^2$ $n_o = n_i \exp[(E_F - E_i) / kT]$ or $(E_F - E_i) = kT \ln(n_o/n_i)$ $p_o = n_i \exp[(E_i - E_F) / kT]$ or $(E_i - E_F) = kT \ln(p_o/n_i)$ $\sigma = q(n\mu_n + p\mu_p)$

* Definitions of parameters are not given for the provided information. It is expected that the examinees interpret the meaning.

Problem : 22

Area: Computational Intelligence

Student Code_____

Describe how machine learning can help with a biomedical application of your choice. Focus particularly on the advantages and disadvantages of the approach(es) you are describing. Briefly outline the technical challenges of your chosen problem. You will be graded primarily on the appropriateness and technical quality of your answer.

Problem : 24

Area: Computational Intelligence

Student Code_____

Describe one of the following in detail (your choice): Long Short Term Memory (LSTM), You Only Look Once (YOLO), Maxout, Dropout, Variational Autoencoder.

a) A program's run time is decided by the product of instructions per program (IC), average clock cycles per instruction (CPI), and clock frequency (f). Assume the following instruction mix for a MIPS-like RISC instruction set: 15% stores, 25% loads, 15% branches, and 35% integer arithmetic, 5% integer shift, and 5% integer multiply. Given that load/store instructions require two cycles, branches requires four cycles, integer ALU instructions require one cycle, and integer multiplies require ten cycles, compute the CPI.

b) Given the same parameters in Question A, consider an optimization that converts multiplies by a compile-time constant into a sequence of shifts and adds. For this instruction mix, 50% of the multipliers can be converted to shift-add sequences with an average length of three instructions. Compute the change in instructions per program (IC), average clock cycles per instruction (CPI), and overall program speed-up.

Problem : P26**Area: Computer Architecture & Embedded Systems****Student Code:_____**

Suppose we have two implementations of the same instruction set architecture. For some program which has 1 million instructions,

Machine A has a clock cycle time of 100ps and an average CPI of 2.0.

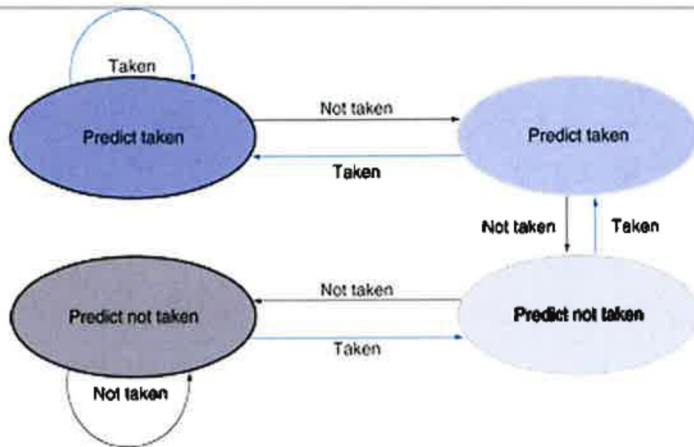
Machine B has a clock cycle time of 130ps and an average CPI of 1.5.

a. What machine is faster for this program, and by how much?

b. If overclocking (i.e., driving the given machine with faster clock) of the slower machine is possible, what clock rate should be used to execute the given program to achieve the same execution time of the faster machine?

Problem : P27**Area: Computer Architecture & Embedded Systems****Student Code: _____**

Calculate the branch prediction accuracy (= # of correct predictions / # of total predictions) of the following branch outcome sequence using the 2-bit predictor shown below. Assume that the initial state is one on bottom-left.



Branch outcome sequence (T means "branch-taken and N means "branch-not-taken"):

T, T, N, N, N, T, N, T, N, T

Problem : P28

Area: Computer Architecture & Embedded Systems

Student Code:_____

Suppose you are given a simple memory hierarchy with a 4-way set associative cache memory which can store 8 one-word data blocks and a word-addressable main memory which can store 16 data words. For a word address sequence of 0000, 1000, 0000, 1000, 1100, 0100 and 1100 in binary, construct a table to show: tag, index, hit/miss and cache contest after each access. Use LRU (Least Recently Used) replacement strategy. Then, calculate its hit ratio.

Problem: P29

Area: Integrated Circuits and Logic Design

Code # _____

Find the minimal SOP expression for f, which is given as:

$$f(w, x, y, z) = (w + y' + z)(w' + x + y' + z')(w' + x' + y' + z)(x + y' + z')(w' + x' + y' + z)(w' + x' + y' + z')$$

Given the function $F(A,B,C,D)$ below. Answer the following questions.

$$F = \prod_{ABCD} M(0,4,6,7,9,10,12,15) + dc(1,2,5)$$

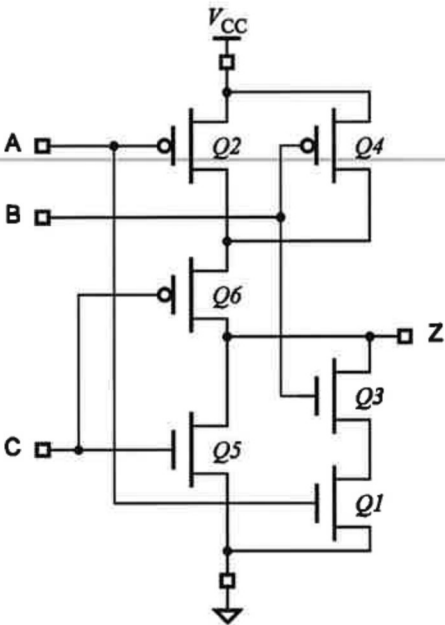
(a) Write the canonical SOP expression for F .

(b) Determine the minimal POS expression for F .

- (c) Determine the minimal SOP expression for F.
-

Answer the questions for parts a and b below.

- a. For the CMOS circuit shown to the right, indicate whether each transistor is ON or OFF and the function output Z (H or L).



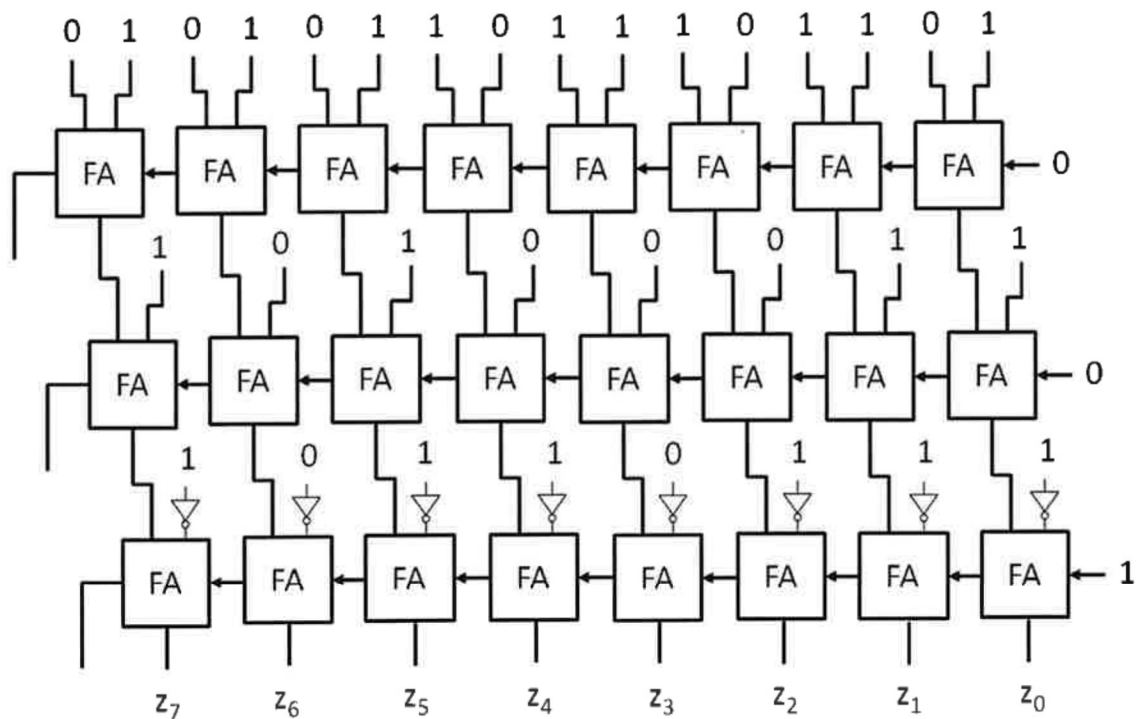
A	B	C	Q1	Q2	Q3	Q4	Q5	Q6	Z
L	L	L							
L	L	H							
L	H	L							
L	H	H							
H	L	L							
H	L	H							
H	H	L							
H	H	H							

- b. Determine the logic function for Z from the CMOS logic circuit in part a.

Answer the following questions.

- a) Implement $Z = 2X - 3Y$ in 8-bit 2's complement using only Full Adders and inverters; assume $X = 00x_5x_4x_3x_2x_1x_0$ and $Y = 00y_5y_4y_3y_2y_1y_0$.

- b) Assume that the delay per sum operation is 4ns, the delay per carry operation is 3ns, and the delay per inverter is 2ns; how long does it take to calculate z_6 ?

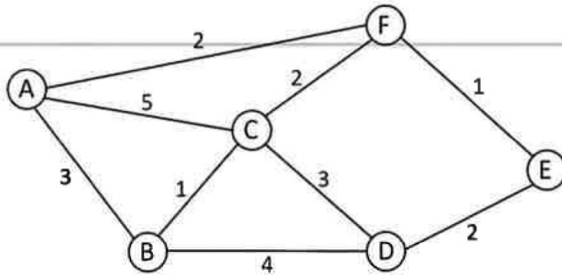


Problem: P33

Area: Networking, Security, and Dependability

Student Code: ____

Consider the network in the figure below. Use Dijkstra's algorithm to identify the shortest paths from node B to all other nodes. Show your work.



Problem: P35

Area: Networking, Security, and Dependability

Student Code: _____

Answer all three questions below. Justify your answers.

1. Given keys of equal length, in general, is asymmetric encryption more, less, or about as secure as symmetric encryption?
2. Recall RSA, where the ciphertext, C , of a plaintext message, M , is generated as $C = M^f \bmod n$, and decryption recovers $M = C^g \bmod n$.

$M < n$ and n is a product of two distinct (and secret) primes, p and q , but n itself is not secret. f and g are chosen such that $\gcd(f, \varphi(n)) = 1$, $1 < f < \varphi(n)$, $f \cdot g \equiv 1 \bmod \varphi(n)$, and $g \equiv f^{-1} \bmod \varphi(n)$.

Is $\{g, n\}$ the public or private key? Justify your answer.

3. In RSA, it is often recommended to choose a small value for f to increase efficiency. A common choice is 3. Why is $f = 2$ not a valid choice?

Problem: P36

Area: Networking, Security, and Dependability

Student Code: _____

Consider sending a file of $F = M \cdot L$ bits over a path of Q links. Each link transmits at R bps. The network is lightly loaded so that there are no queuing delays. When a form of packet switching is used, the $M \cdot L$ bits are broken up into M packets, each packet with L bits. Propagation delay is negligible.

Answer all three questions below.

1. Suppose the network is a packet-switched virtual circuit network. Denote the setup time of the virtual circuit by t_s seconds. Suppose the sending layers add a total of h bits of header to each packet. How long does it take to send the file from source to destination?
2. Suppose the network is a packet-switched datagram network and a connectionless service is used. Now suppose each packet has $2h$ bits of header. How long does it take to send the file?
3. Finally, suppose that the network is a circuit-switched network. Further suppose that the transmission rate of the circuit between source and destination is R bps. Assuming t_s seconds of setup time and h bits of header appended to the entire file, how long does it take to send the file?